PowerCard
Methodologies for Designing Power-Aware Smart Card Systems

Project Goal

To develop new methodologies for designing and implementing entire systems with regard to power-awareness and required performance

PowerCard Tool Demos

Functional platform design example
Modeled in C/C++ with interface based communication
SystemC™ is used as simulation engine
Functional model to architecture model mapping is performed by the user via the graphical user interface
Refined simulation models will be generated automatically
Virtual prototypes enable rigorous verification and testing
Additional tools perform energy estimation and optimization

Cycle-accurate software energy analysis is provided
Power profile can be viewed in detail
Function level energy reports give feedback to designers
Instruction-level code optimization for low energy is done automatically
Energy estimation and optimization has been integrated in standard software development tools
Demonstration for a DES algorithm implementation

Java Card™ virtual machine processor
RISC-based stack architecture
Software development tool-chain
Assembler with formal stack verification
Mixed Java/Assembly implementation of runtime environment
Security features supported by hardware
Proven against memory attacks

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